

2133

PATENT

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: YU-CHUAN CHANG AND XUE-NING REN

Serial No: 09/262,960

Attorney Docket No: TD9907IN

Filed: 03/04/99

Group Art Unit: 2133

METHOD AND MODULE FOR UNIVERSAL  
TEST OF COMMUNICATION PORTS

Examiner: CHUNG, P

**AMENDMENT RESPONSIVE TO OFFICE ACTION**  
**MAILED 10/02/01**Honorable Commissioner of Patents and Trademarks  
Washington, D.C. 20231**022192**

PATENT AND TRADEMARK OFFICE

Sir:

Transmitted herewith for filing is Applicant's Response to Office Action. Should the Examiner have any question, he or she is invited to call or fax the undersigned at the telephone numbers indicated below. If, for any reason, this Response is not timely filed, this is a petition for extension of time as necessary for timely filing, and the Commissioner is authorized to charge any necessary statutory fees to Charge Account No. 50-1260.

Respectively Submitted,

01/02/02

Date

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**RECEIVED****FEB 28 2002****Technology Center 2100****CERTIFICATE OF MAILING (37 CFR §1.8a)**

I hereby certify that this paper (along with any documents referred as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelop addressed to: The Commissioner of Patents and Trademarks, Washington, D.C., 20231.

W. Wayne Liauh  
(Type or print name of person mailing paper)01/02/02  
Date  
(Signature of person mailing paper)

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✓D  
3-2-02

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Honorable Commissioner of Patents and Trademarks  
Washington, D.C. 20231

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AMENDMENT

In response to the Office Action mailed on 10/02/01, please amend the above-identified application as follows:

In the Specification:

Please amend the following portions of the Specification as shown:

On page 7, lines 12-17:

As shown in FIG. 3, the testing module 10 connects both parallel port 21 and serial port 22 of the computer 20. The logic control unit 11 provides four [pair] pairs of 8-bit input/output ports for transmitting and receiving control or data signals. In other words, there are  $4 \times 8 = 32$  input/output lines for controlling and reading signals of all pins of the parallel port 21 and the serial port 22 and detecting the open or short circuit condition. The detailed connection of the pins and ports are shown